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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/550,282	04/14/2000	Sung-Il Park	1607-0211P	9574

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EXAMINER	
QI, ZHI QIANG	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/550,282	PARK ET AL.	
	Examiner	Art Unit	
	Mike Qi	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2004 and 19 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6,9-15,17 and 19-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,9-15,17 and 19-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on Sep.22, 2004 and Oct.19, 2004 has been entered.

Claim Objections

1. Claims 15, 22 and 26 are objected to because of the following informalities:

Claim 15, recitation ". . . forming an insulating layer electrically insulating said gate line and the gate electrode;. . ." in which the gate electrode is connected with the gate line, so that an insulating layer electrically insulating the gate line and the gate electrode is not correct. For examination purpose, it should be an insulating layer electrically insulating the data line from the gate line.

Claim 22, recitation ". . .forming a low reflective layer over at least a portion of at least one of said gate line and said data line and on the first and second regions; . . ." in which the first and second region do not have the definition in the claim. For examination purpose, the first region and the second region should be the first portion of the semiconductor layer (source area) and the second portion of the semiconductor layer (drain area).

Claim 26, recitation ". . . a source electrode and a drain electrode connected to the drain line. . ." in which according to the Figs.5-6, both of the source electrode and the drain electrode cannot be connected to the drain line. For examination purpose, the source electrode is connected to the data line and the drain electrode is connected to the pixel electrode.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 11, 14-15, 22 and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,259,200 (Morita et al).

Claims 1, 15 and 22, Morita discloses (col.5, lines 59 – col.6, line 65; Figs.5-6) that a liquid crystal display device comprising:

(concerning claims 1 and 15)

- gate line (43) formed on a transparent substrate (1), and gate electrode (G) of the TFT (3) to be connected with the gate line (43) on the transparent substrate (1);
- signal line (10) (data lines) crossing the gate line (43) and formed on the transparent substrate (1); and the data line (10), source electrode and

drain electrode over the transparent substrate (1), the source electrode and the drain electrode being respectively disposed in source area (7) and drain area (8), and the source electrode being connected with the data line (10) through contact hole (S);

- gate insulating layer (4a,4b) electrically insulating the data line (43) from the gate line (10);
- thin film transistor (TFT) (3) formed at an intersection of the gate line (43) and the data line (10), and connected to the gate line (43) and the data line (10), and the TFT being disposed in an area having a channel area (between the source area and the drain area), a source area (7) and a drain area (8); and the TFT (3) having gate electrode, source electrode and drain electrode;
- planarization film (12) made of organic resin that functions as passivation layer (col.4, lines 31-32) formed over the TFT (3);
- pixel electrode (14) having portions formed on the surface of the planarization film (12) (functions as a passivation layer), but not over the TFT (3);

(concerning claim 22)

- forming a gate line (43) and gate electrode (G) connected thereto on a transparent substrate (1),
- forming gate insulating film (4a,4b) over the gate line (43) and the gate electrode (G);

- forming a semiconductor layer (2) over the gate electrode (G);
- forming a signal line (10) (date line) crossing the gate line (43); and a source electrode connected to the data line (10) through contact hole (S) and on a first portion (source area) (left portion) of the semiconductor layer (2), and a drain electrode on a second portion (drain area) (right portion) of the semiconductor layer (2);
- forming planarization film (12) (functions as a passivation layer) having a contact hole exposing the drain electrode over the transparent substrate (1);
- forming pixel electrode (14) with portions disposed on the planarization film (12) (functions as a passivation layer), but not over the TFT, and connected to the drain electrode via the contact hole.

Morita does not expressly discloses in the Figs.4-6 that a low reflective layer formed on at least a portion of the gate line or the data line; and no black matrix between the pixel electrode and the upper substrate and above the low reflective layer.

However, Morita discloses (col.4, lines 51-67; Fig.2) that the signal line (10) is manufactured of a metal film having relatively high reflectance, and another metal film (10x) having relatively low reflectance is formed on top of the first metal film; and there is no black matrix between the upper substrate (60) and the pixel electrode (14) in the Fig.2. Because the low reflective layer (10x) is formed on the signal line (10), so that the area does not have black matrix also is above the low reflective layer (10x). Morita indicates (col.4, lines 62 – 67) that the top layer of the signal lines (10) of Al will cause

its reflectance to be large enough to degrade the quality of image, such that a top layer of material having a relatively low reflectance is further applied on the Al film to preclude unwanted light reflection. Because the low reflective layer having the function of light shielding, so that the light would be shielded to pass the signal line. For the same reason, using the low reflective layer to cover the gate line, the source area, drain area and channel region that would shield the light passing the gate line and the channel area, source area and drain area.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to arrange a low reflective layer on the data line or on the gate line, and on the channel area, source area, drain area, and no black matrix between the pixel electrode and the upper substrate as claimed in claims 1, 15 and 22 for precluding the unwanted light reflection.

Claim 11, Morita discloses (col.5, lines 59 – col.6, line 65; Figs.5-6) that the planarization film (functions as passivation layer) formed over the gate line (gate electrode connected to the gate line 43), the data line (the source electrode connected to the signal line 10), the low reflective layer (such as the low reflective layer 10x on the signal line 10); and the pixel electrode (14) formed on the planarization film (12) (functions as passivation layer); and the pixel electrode (14) is connected to the TFT via a contact hole in the planarization film (12) (functions as passivation layer).

Claims 14 and 25, Morita discloses (col.7, lines 14-25; Fig.6) that a color filter (63) is formed on the color filter substrate (60); and liquid crystal (50) sealed between the color filter substrate (60) and transparent substrate (1).

Claim 26, Morita discloses (col.5, lines 59 – col.6, line 65; Figs.5-6) that the thin film transistor (TFT) includes:

- gate electrode (G) connected to the gate line (43); and the gate electrode (G) being covered with the channel region (between the source area 7 and the drain area 8);
- source electrode is connected to the data line (signal line 10), drain electrode is connected to the pixel electrode (14); and the source electrode and the drain electrode being respectively covered with the source region (7) and the drain region (8).

FIG. 6

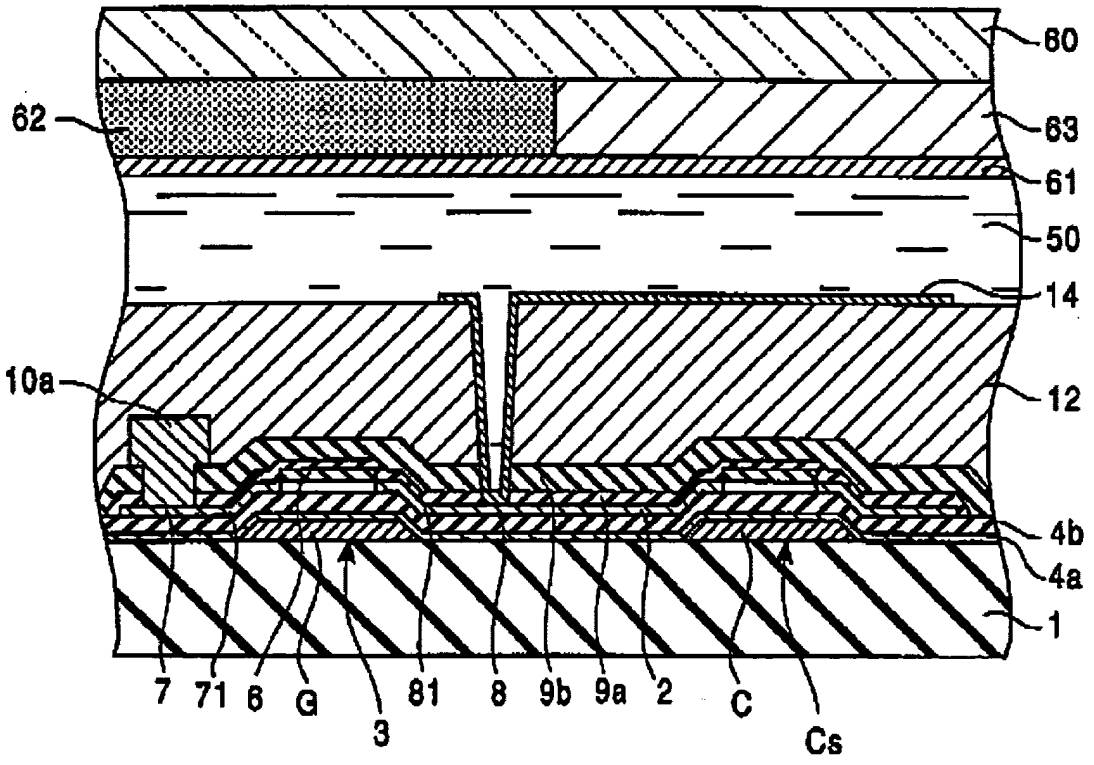
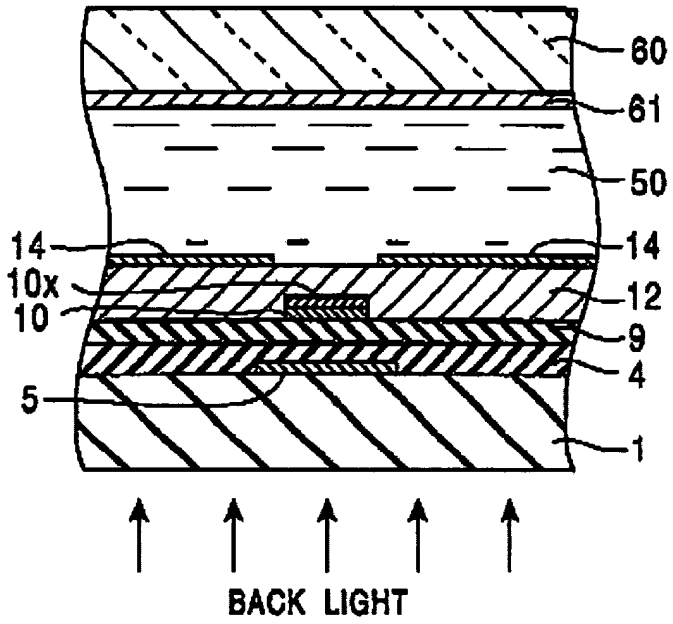


FIG. 2



4. Claims 12-13 and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morita as applied to claims 1, 11, 14-15, 22 and 25-26 above, and further in view of US 6,172,728 (Hiraishi).

Claims 12-13 and 23-24, lacking limitation is such that the pixel electrode is formed over (or overlap) a portion of the data line or a portion of gate line.

However, Hiraishi discloses (col.5, lines 56-57; Fig.1) that the pixel electrode (4) is formed over (or overlap) a portion of the data line (3) and a portion of the gate line (2), and the unnecessary leakage of light to the gap between the pixel electrodes and the gate lines or the date lines are prevented.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to arrange the pixel electrode overlap a portion of the gate line or

the data line as claimed in claims 12-13, 23-24 for preventing the unnecessary light leakage to the gap between the pixel electrodes and the gate lines or the date lines.

5. Claims 5-6, 9-10 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morita as applied to claims 1, 11, 14-15, 22 and 25-26 above, and further in view of US 6,172,728 (Hiraishi) and Applicant admitted prior art (AAPA).

Claims 5-6, 9-10 and 20-21, lacking limitation is such that the low reflective layer is formed of CrOx (claims 6,10 and 21), and the low reflective layer has a light reflectivity of 3% or less (claims 5, 9 and 20).

However, Hiraishi discloses (col.6, lines 34-37; Fig.1) that by providing a low-reflective film preferably made of chromium oxide (CrOx) on the gate lines (2) and the source lines (3) (data line), the display quality is enhanced.

Concerning the low reflective layer has a light reflectivity of 3% or less that is the property of the material (CrOx), and the same material must have the same property, and that would have been at least obvious. Furthermore, AAPA indicates (page 4, lines 2-3 of the specification) that the material of CrOx is widely used for black matrix to reduce the influences of the light reflection because the reflectivity of CrOx is about 3%. Therefore, the property of the CrOx (reflectivity is about 3%) must be widely known in the art.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to use the material of CrOx as the low reflective layer (reflectivity about 3%) as claimed in claims 5-6, 9-10 and 20-21 for enhancing the display quality.

Note: Claim 9 is the same as the claim 5, and Claim 10 is the same as the claim 6. Therefore, claims 9 and 10 are redundant.

6. Claims 3-4, 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morita as applied to claims 1, 11, 14-15, 22 and 25-26 above, and further in view of US 6,172,728 (Hiraishi) and US 6,172,723 (Inoue et al).

Claims 3-4, 17 and 19, lacking limitation is such that the low reflective layer is formed on (or cover) the gate electrode or on the source and drain electrodes.

However, Hiraishi discloses (col.6, lines 34-37; Fig.1) that by providing a low-reflective film preferably made of chromium oxide (CrOx) on the gate lines (2) (the gate electrode is connected to the gate line) and the source lines (3) (data line) (the source electrode is connected to the data line), the display quality is enhanced. Therefore, forming a low reflective layer on the gate electrode and on the source/drain electrode to enhancing the display quality would have been at least an obvious variation.

As an evidence, Inoue discloses (col.1, lines 45-51) that lights are mixed with light reflected from the reflection electrode and this mixed light lowers the image display quality. Inoue indicates (col.11, lines 34-50) that in order to solve such problem, a low reflection conductive film is patterned on the high reflection conductive film. The gate electrode, source electrode and drain electrode are electrical conductive film. Therefore, those skilled in the art would be benefited from those prior art to form a low reflective layer patterned on an electrode such as the gate electrode and source/drain electrode to enhance the image display quality.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to arrange a low reflective layer on the electrodes as claimed in claims 3-4, 17 and 19 for enhancing the image display quality.

Response to Arguments

7. Applicant's arguments with respect to claims 1,3-6,9-15,17,19-26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1) US 6,061,110 (Hisatake et al) discloses (col.3, lines 46 – 61) that in order to increase the brightness of the reflective liquid crystal display device, no light shielding layer is applied. According to the low reflective layer (such as the material Cr/CrOx having same function as black matrix) formed over the gate line or date line that will suppress the reflectance, such that the black matrix is not required so as to increase the display brightness.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Qi whose telephone number is (571) 272-2299. The examiner can normally be reached on M-T 8:00 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mike Qi

Mike Qi
Patent Examiner